Improvement in electron holographic phase images of focused-ion-beam-milled GaAs and Si *p-n* junctions by *in situ* annealing

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Low temperature (200–600 °C) annealing in the transmission electron microscope (TEM) is used to provide a significant noise reduction in phase images of focused-ion-beam-milled GaAs and Si *p-n* junctions recorded using off-axis electron holography, as well as increasing the measured phase shifts across the junctions. Our results suggest that annealing removes defects resulting from Ga^+ implantation and reactivates dopant atoms in the thin TEM specimens. In GaAs, electrically inactive surface layer thicknesses are reduced from 80 to 17 nm on each specimen surface after annealing at 500 °C. In Si the improvement is from 25 to 5 nm. © *2006 American Institute of Physics.*
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Off-axis electron holography promises to fulfill the requirements of the semiconductor industry[1] for a technique that can be used to provide quantitative information about dopant potentials in semiconductors with nanometer spatial resolution. The technique uses an electron biprism in a transmission electron microscope (TEM) to interfere a coherent electron wave that has passed through a specimen with a reference wave that has passed through vacuum. In the absence of magnetic fields, the phase shift of the electron wave that has passed through the specimen is given by the expression

$$\varphi(x,y) = C_E \int_{-\infty}^{\infty} V(x,y,z)dz, \quad (1)$$

where C_E is a constant dependent on the energy of the electron wave, V is the electrostatic potential and z is the electron beam direction.[2] In a specimen of uniform thickness, the phase shift is expected to provide a quantitative measure of the variation in potential associated with the presence of dopant atoms. However, TEM specimen preparation can have a profound influence on phase shifts measured from doped semiconductors.[3] In addition to surface depletion resulting from the presence of the specimen surfaces, the potential in the specimen may be affected by oxidation, damage and the implantation of Ar and Ga ,[4] as well as by irradiation by high-energy electrons during TEM examination.[5]

Focused ion beam (FIB) milling is now routinely used to prepare semiconductor devices for electron holography due to its site specificity, as well as the ease with which a specimen of uniform thickness can be prepared. Here, we show that *in situ* annealing of doped semiconductors prepared for TEM examination using FIB milling with Ga^+ increases the phase shift measured across *p-n* junctions in GaAs and Si, while at the same time decreasing noise in the recorded phase images.

TEM specimens of uniform thickness containing GaAs and Si *p-n* junctions were prepared for electron holography using an FEI 200 FIB workstation operated at 30 kV. The GaAs *p-n* junction was grown using molecular beam epitaxy (MBE), and comprised a 1.0-μm-thick 1×10^{18} cm^{-3} Si-doped (*p*-type) layer on a 1.0-μm-thick 1×10^{18} cm^{-3} Be-doped (*n*-type) layer on an undoped GaAs (001) substrate. The Si *p-n* junction was also grown using MBE, and comprised a 2.5-μm-thick 5×10^{18} cm^{-3} B-doped (*p*-type) layer on a 4×10^{18} cm^{-3} Sb-doped (*n*-type) (001) substrate. Parallel-sided electron-transparent membranes were FIB milled from each wafer in "trench" geometry,[6] with final thicknesses of between 200 and 700 nm. A Pt strap was deposited over the area of interest to protect the specimen from Ga^+ implantation and damage during FIB milling. A "cut" was made in each membrane to provide a region of vacuum close to the junction for holography.[7] Care was taken to minimize Ga^+ implantation by exposing the region of interest only at a glancing angle to the ion beam. Final thinning was performed using a low beam current (150 pA).

Electron holograms were acquired at 200 kV in a Philips CM300-ST field-emission gun TEM, equipped with a rotatable electron biprism and a 2048 pixel charge-coupled device camera. A Lorentz minilens was used as the imaging lens for electron holography, with the conventional microscope objective lens switched off. A biprism voltage of 100 V was used to provide a holographic overlap width of ~750 nm and an interference fringe spacing of 5 nm. Specimens were tilted by a few degrees from ⟨110⟩ to minimize diffraction contrast. Prior knowledge that the wafer miscut angles were below 0.1° from (001) was used to ensure that each junction was edge-on with respect to the electron beam. Reference holograms were acquired from vacuum after each hologram of the specimen and used to remove geometrical distortions associated with the imaging and recording system.[9]

Each sample was heated *in situ* in the TEM to temperatures of 200, 300, 400, 500, and 600 °C for 1 h, with a period of 30 min at room temperature between each elevated

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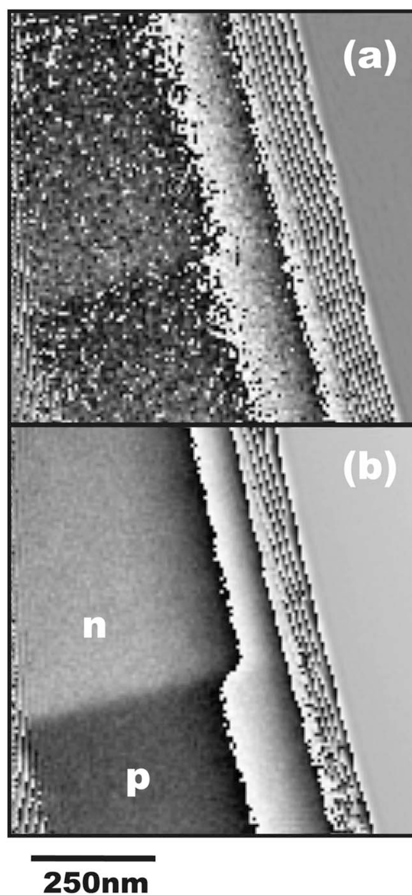

FIG. 1. Wrapped electron holographic phase images of a FIB-milled GaAs *p-n* junction of crystalline thickness 240 nm, recorded at (a) room temperature and (b) after *in situ* annealing at 500 °C. In each image, black and white correspond to $-\pi$ and $+\pi$ radians, respectively.

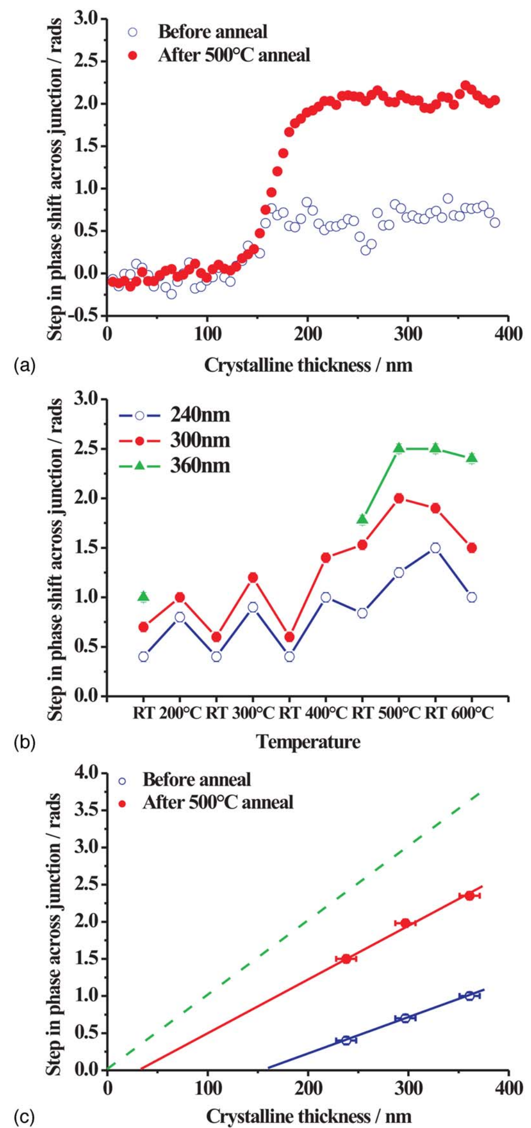

FIG. 2. (Color online) (a) Phase profiles measured across a FIB-milled GaAs *p-n* junction in a sample of crystalline thickness 300 nm, before (open circles) and after (closed circles) *in situ* annealing at 500 °C. The profiles are averaged over a distance of 120 nm on the specimen. (b) Shows the effect of successive annealing and cooling on the step in the measured phase shift across the junction. The horizontal axis shows the temperature at which each measurement was made. The specimens were heated for one hour and cooled for 30 min before each hologram was acquired. The legend lists the different crystalline specimen thicknesses examined. (c) The phase shift across the junction plotted as a function of crystalline specimen thickness before (open circles) and after (closed circles) annealing at 500 °C. The values that would be expected from the nominal bulk properties of the specimen are shown using a dashed line.

temperature. Holograms were acquired at room temperature and at elevated temperatures. The specimens were believed to have reached thermal equilibrium when no specimen drift was observed. The crystalline thickness of each specimen, which was unchanged after annealing to within experimental error, was measured to a precision of ±10 nm using convergent-beam electron diffraction.

Figure 1 shows wrapped phase images from a 240-nm-thick GaAs *p-n* junction, acquired at room temperature before and after annealing at 500 °C. A dramatic increase in the phase shift, $\Delta\varphi$ across the junction and a decrease in noise in the specimen after annealing are visible in the images. The improvement is shown more quantitatively in Fig. 2(a), in the form of phase profiles measured across the same *p-n* junction, this time for a 300-nm-thick specimen. In this specimen, $\Delta\varphi$ increases from 0.70 ± 0.10 rad at room temperature to 2.00 ± 0.05 rad after annealing at 500 °C.

As a result of poor signal to noise, not all of the holograms that were acquired from the thickest (360 nm) membrane could be reconstructed successfully until annealing had been used to improve the phase images in the manner shown in Fig. 1. Figure 2(b) shows the effect of annealing on three GaAs *p-n* junction specimens. When measured at elevated temperature, $\Delta\varphi$ increases with temperature up to 500 °C. Initially, after heating to either 200 or 300 °C and subsequent cooling, the starting room temperature value of $\Delta\varphi$ is recovered. However, after annealing at temperatures of 400 or 500 °C and subsequent cooling, $\Delta\varphi$ increases substantially from its initial value measured after specimen preparation. $\Delta\varphi$ measured at room temperature is maximized after annealing at 500 °C.

Figure 2(c) shows $\Delta\varphi$ plotted as a function of crystalline specimen thickness. By extrapolating these measurements to lower specimen thickness, a value for $\Delta\varphi$ of zero is predicted to occur at a crystalline specimen thickness of 160 ± 10 nm before annealing, and 34 ± 10 nm after annealing. These values are assumed to correspond to approximately twice the crystalline electrically "inactive" layer thickness on *each* specimen surface, i.e., 80 ± 5 nm and 17 ± 5 nm before and after annealing, respectively. The definitions of these layers are discussed in more detail elsewhere.[3,6]

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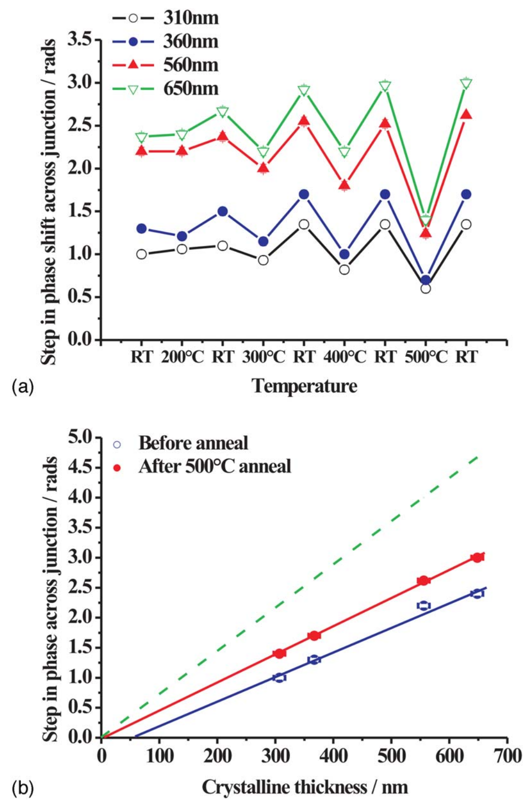

FIG. 3. (Color online) (a) and (b) As for Figs. 2(b) and 2(c) but for Si rather than GaAs *p*-*n* junctions.

Figure 3 shows corresponding results obtained from FIB-prepared Si *p*-*n* junctions. In Fig. 3(a), the room temperature value of $\Delta\varphi$ increases after annealing at temperatures of 300, 400, and 500 °C (from the value measured immediately after specimen preparation), although this increase in not as pronounced as for GaAs in Fig. 2.

The most significant difference between Figs. 2(b) and 3(a) is that, for Si, $\Delta\varphi$ measured at elevated temperature decreases with increasing temperature, whereas an increase was observed for GaAs. At the temperatures considered here, both Si and GaAs are expected to be in their intrinsic regimes, where the intrinsic carrier concentration increases rapidly with temperature. The Fermi levels in the *p*- and *n*-type regions then move closer to the intrinsic Fermi level, reducing the built-in voltage. The discrepancy observed for GaAs may result from the presence of defects in the band gap that extend the extrinsic regime to higher temperature by reducing the intrinsic carrier density.

Extrapolation of Fig. 3(b) to determine the crystalline specimen thickness for which $\Delta\varphi=0$ suggests that the electrically inactive surface layer thicknesses on the Si specimens are reduced from 25 ± 5 nm to 5 ± 5 nm after annealing at temperatures of 300–500 °C.

On the assumption that a *p*-*n* junction is only present throughout the electrically active thickness of the specimen t_{el}, the built-in voltage across the junction can in principle be measured by using the equation

$$V_{bi}=\frac{1}{C_E}\cdot\frac{\Delta\varphi}{t_{el}}. \quad (2)$$

The application of Eq. (2) to the graphs shown in Figs. 2(c) and 3(b) provides values for V_{bi}, before annealing, of 0.67 ± 0.10 V and 0.55 ± 0.10 V in the GaAs and Si specimens, respectively. The corresponding measurements are 1.00 ± 0.10 V and 0.65 ± 0.10 V after annealing at 500 °C for GaAs and 300 °C for Si, respectively. Although a decrease in the electrically inactive surface layer thickness is observed on annealing, further work, including comparisons with simulations of dopant potentials in thin specimens, is required to understand the remaining discrepancy with the expected values for V_{bi} (1.38 V for GaAs and 0.95 V for Si). Factors to consider include residual ion damage and doping of the specimen surfaces, irradiation by the electron beam, and interdiffusion of dopant atoms on annealing.

Recent studies on doped GaAs have shown that defects resulting from Ga^+ implantation, which can pin the Fermi level within the band gap,[8] have been detected at depths below the specimen surface in excess of 300 nm,[9] many times larger than suggested by simulation programs.[10] The difficulty of understanding the behavior of such defects with temperature is highlighted by the fact that in GaAs, defects that pin the Fermi level 0.34, 0.59, and 0.70 V below the conduction band are removed at temperatures of between 210 and 420 °C.[10,11] Similarly, in Si, defects that pin the Fermi level at energies of 0.23, 0.30, and 0.38 V above the valence band are removed at temperatures of between 300 and 400 °C.[12] Such effects may need to be included in simulations of TEM specimens to reproduce the results presented in Figs. 2 and 3 quantitatively.

In summary, the present study suggests that approaches such as *in situ* annealing may ultimately allow the site specificity of FIB milling to be combined with the quantitative nature of electron holography to provide meaningful and reliable information about the electrical properties of semiconductor devices with nanometer spatial resolution. However, the remaining discrepancies between predicted and experimental results must be overcome or understood fully before the technique can be applied routinely with confidence.

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