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Quantitative off-axis electron holography of GaAs *p-n* junctions prepared by focused ion beam milling

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Summary

Focused Ion beam (FIB) prepared GaAs *p-n* junctions have been examined using off-axis electron holography. Initial analysis of the holograms reveals an experimentally determined built-in potential in the junctions that is significantly smaller than predicted from theory. In this paper we show that through combinations of *in situ* annealing and *in situ* biasing of the specimens, by varying the intensity of the incident electron beam, and by modifying the FIB operating parameters, we can develop an improved understanding of phenomena such as the electrically 'inactive' thickness and subsequently recover the predicted value of the built-in potential of the junctions.
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Introduction

Off-axis electron holography is a TEM-based technique that uses a biprism to interfere an object wave that has passed through a specimen with a reference wave that has passed through only vacuum. From the interference pattern, known as an electron hologram, a phase image and an amplitude image of the specimen can be reconstructed. In the absence of magnetic fields and diffraction contrast, the phase change of an electron as it passes through a specimen of thickness, t is given by;

$$\Delta\phi = C_E \int_0^t V(x, y, z)dz \qquad (1)$$

where C_E is a constant dependent on the energy of the electron wave, V is the electrostatic potential and z, the electron beam direction (Tomomura, 1982).

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As the electrostatic potential of a material is very sensitive to changes in semiconductor specimens, such as from presence of dopants, off-axis electron holography promises to fulfill the requirements of the semiconductor industry (ITRS, 2007) for a technique that can provide both 2D and 3D maps of the electrostatic potential in nanometer-scale devices (McCartney *et al.*, 1994; Rau *et al.*, 1999; Gribelyuk *et al.*, 2002, 2008; Twitchett *et al.*, 2007).

Figure 1 shows a schematic for off-axis electron holography. The field emission gun (FEG) is a source of coherent electrons. By applying a voltage to the biprism, two virtual sources, S_1 and S_2, are formed in the back-focal plane that forms an interference pattern in the image plane. This interference pattern is then processed to provide phase and amplitude images of the specimen (Volkl *et al.*, 1999).

It can be shown that the maximum spatial resolution in the phase image is three times the fringe spacing of the hologram. By increasing the voltage on the biprism, the virtual sources can be pushed further apart, which has the dual benefit of both reducing the fringe spacing and increasing the interference width of the hologram to provide a larger field of view. However, the increasing width of the interference pattern places higher constraints upon the coherence of the electrons, which reduces the contrast, μ of the hologram. As the resolution of a phase image can be described using the expression:

$$\Delta\phi = \frac{\sqrt{2}}{\mu\sqrt{N}} \qquad (2)$$

where N is the number of counts in the reconstructed phase image (Harscher *et al.*, 1996), it is evident that a loss of the contrast of the hologram will lead to a reduction in the resolution of the phase image. The stability of the microscope will determine the length of acquisition time that can be used to optimise N without compromising the hologram contrast. In practice a compromise between contrast, spatial resolution

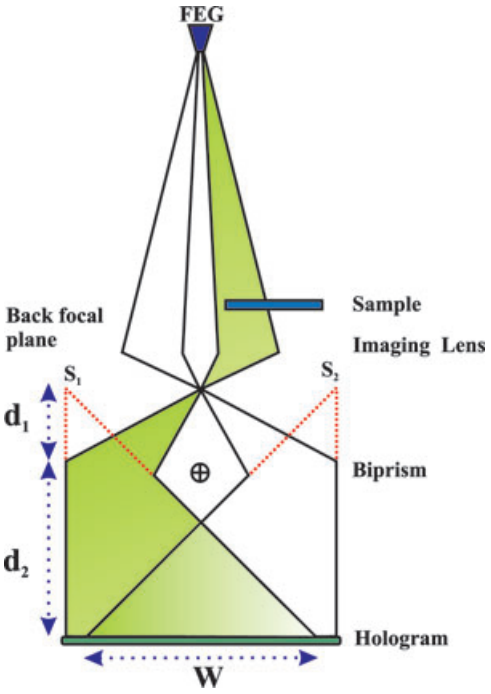

Fig. 1. Schematic showing how electron holograms of width, *W* are formed by using a charged biprism.

and image acquisition time is required to acquire a hologram with the optimum amount of information for each specific experiment (Lichte, 2007).

By using the focused ion beam and advanced specimen preparation procedures such as *in situ* lift out (Overwijk *et al.*, 1993), specimens that contain semiconductor devices can be prepared with relative ease and phase images can be reconstructed that reveal the dopant-related variations in electrostatic potential. However, quantitative dopant profiling is more difficult, especially in the case of device specimens where combinations of artifacts from FIB specimen preparation and specimen charging make direct measurement of the dopant concentrations complicated (Dunin *et al.*, 2005; Twitchett *et al.*, 2002, 2004; Lenk *et al.*, 2005).

To understand the origins of the artifacts that are observed when FIB-prepared *p-n* junctions are examined using off-axis electron holography, the experiment has been simplified as much as possible by growing simple symmetrically doped GaAs *p-n* junctions for analysis.

Direct measurement of the built in potential in the *p-n* junctions using off-axis electron holography

The GaAs *p-n* junctions examined in this study were grown using molecular beam epitaxy (MBE) and comprised a 1.0-μm-thick, 1×10^{18} cm^{-3} Be-doped (*n*-type) layer grown onto a 1.0-μm-thick, 1×10^{18} cm^{-3} Si-doped (*p*-type) layer on an undoped GaAs (001) substrate. Theoretically, the built-in potential, V_{bi} across the *p-n* junction is 1.34 V after accounting for the effects of degeneracy (Gibbons *et al.*, 1975). Three different specimens were prepared for examination using a nominally identical procedure. Parallel-sided electron-transparent membranes were prepared using a FIB operated at 30 kV using conventional 'trench' geometry (Park, 1990). A platinum layer was deposited over the area of interest using ion beam assisted deposition (IBAD) to protect the specimen both from normal incidence Ga ion implantation and from the tails of the beam. Care was taken to minimize Ga+ implantation by exposing the region of interest only at a glancing angle to the ion beam. Final thinning was performed using a low beam current. The specimens had final crystalline thicknesses in the range 200 to 550 nm that were measured using convergent beam electron diffraction (CBED).

Electron holograms were acquired using 200 kV electrons in a Philips CM300-ST field emission gun TEM, equipped with an electron biprism and a 2048 pixel charge-coupled device camera (CCD). A Lorentz mini-lens was used as the imaging lens with the conventional objective lens switched off. The electron beam was adjusted to be elliptically perpendicular to the biprism in order to maximize the intensity of coherent electrons that were recorded in the hologram. The electron biprism was operated at 100 V providing an interference fringe spacing of 5 nm and therefore a spatial resolution of 15 nm in the reconstructed phase image. The hologram contrast was approximately 20%. The specimens were tilted a few degrees from <110> to minimize diffraction contrast whilst at the same time ensuring that the junctions were kept edge on with respect to the electron beam. Reference holograms were recorded immediately after each hologram of the specimen in order to remove the geometrical distortions associated with the imaging and recording system. For each acquisition, the intensity of the electron beam was minimized to reduce the effects of charging, whilst ensuring that phase images could be reconstructed with a sufficient signal-to-noise ratio to measure the step-in phase across the junctions. The holograms were reconstructed using the software package SEMPER and code developed by Rafal Dunin-Borkowski at the University of Cambridge.

Holograms that showed clearly the presence of the junction were difficult to acquire, especially in thin membranes, while long acquisition times were used to improve the signal-to-noise in the thicker membranes. In all instances the signal-to-noise ratio in the phase images was poor resulting in large errors in the measurement of the step-in phase across the *p-n* junctions. The theoretical phase resolution in the vacuum regions on the phase images was calculated to be only $2\pi/150$ rads for a spatial resolution of 15 nm suggesting that the poor signal-to-noise ratio was due to damage in the specimen rather than from the operation of the microscope.

Figure 2(a) shows a phase image of a 400-nm-thick specimen revealing the differently doped regions of the *p-n*

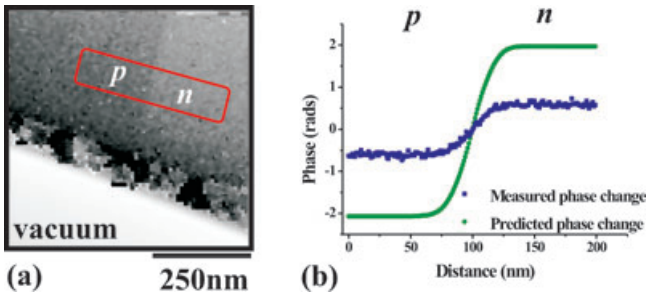

Fig. 2. (a) Phase image containing a 400-nm-thick parallel-sided GaAs *p-n* junction. (b) Phase profile averaged over 100 nm from which the step-in phase across the *p-n* junction is determined.

junction. To measure the value of the V_{bi} in the junction, a phase profile, averaged across 100 nm of the specimen from a region of constant thickness was extracted from the phase image. A value of V_{bi} was then calculated using Eq. (3), where t_{cryst} is the crystalline specimen thickness measured using CBED. The presence of an amorphous layer on the surfaces of specimens prepared in the FIB is well documented (Rubanov *et al.*, 2004, 2005). However, CBED measures only the crystalline thickness of the specimen and the amorphous layers are not accounted for when using the phase to directly calculate V_{bi} across the *p-n* junctions. It has been assumed that the dopants are not active in the amorphous regions of the specimens.

$$\Delta\phi = C_E V_{bi} t_{cryst}. \tag{3}$$

A large discrepancy is observed between the theoretical value of V_{bi} and the experimental measurement. For example, in a 400-nm-thick specimen, a value for V_{bi} across the junction of ~0.4 V is measured which is considerably less than the predicted value of 1.34 V. No detectable phase change was measured in a 200-nm-thick specimen.

Figure 3 shows the step-in phase measured across the three different *p-n* junction specimens as a function of the specimen thickness measured using CBED. The specimens, labelled 'A', 'B' and 'C' were prepared from the same wafer using an identical procedure. The theoretical values that would be expected from a bulk specimen are shown using a dashed line.

From the *x*-intercept, the presence of an electrically 'inactive' thickness that does not contribute towards the total phase measured across the junction is revealed. Clearly the presence of this electrically 'inactive' thickness will result in a reduction of the measured value of V_{bi} across the junctions. Figure 3 shows that for these GaAs specimens the total electrically 'inactive' thickness is in the range 160 to 184 nm corresponding to 80 to 92 nm on each specimen surface. Therefore, in a 400-nm-thick GaAs *p-n* junction specimen, less than half of the total thickness will contribute towards the measured V_{bi}, resulting in a poor signal-to-noise ratio and a

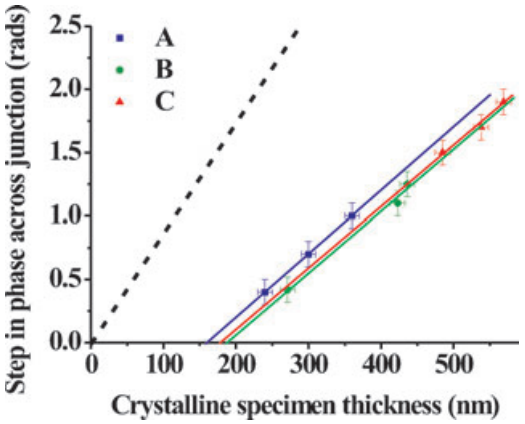

Fig. 3. Step-in phase measured across GaAs *p-n* junctions as a function of total crystalline specimen thickness measured using CBED for specimens A, B and C, prepared at different times from the same wafer. The values that would be expected theoretically from a bulk-like specimen are shown using a dashed line.

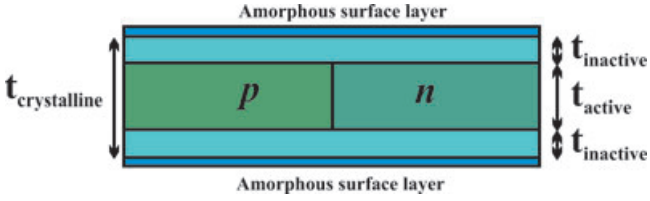

Fig. 4. Schematic diagram showing a thin TEM specimen containing a *p-n* junction. The crystalline thickness is measured using CBED. The total electrically 'inactive' thickness does not contribute towards the measured phase change across the junction. Therefore, in a direct measurement the values of V_{bi} that are obtained are much less than predicted by theory.

Table 1. V_{bi} measured for the GaAs *p-n* junctions and the total thickness of the electrically 'inactive' layers for specimens A, B and C.

Specimen	V_{bi}/V	$t_{inactive}$/nm
A	0.67 ± 0.10	160 ± 15
B	0.66 ± 0.10	184 ± 15
C	0.65 ± 0.10	164 ± 15

large discrepancy between the experimentally determined and theoretical values of V_{bi}. A schematic of a thin TEM specimen containing a *p-n* junction is shown in Fig. 4.

In principle a value for V_{bi} in a *p-n* junction can be calculated independently of the electrically 'inactive' thickness by using Eq. (4).

$$V_{bi} = \frac{1}{C_E} \cdot \left(\frac{\Delta\phi}{t_{crystalline} - t_{inactive}} \right). \tag{4}$$

Table 1 shows the values of V_{bi} and the electrically 'inactive' thickness calculated for the three different specimens.

Although this method of measuring V_{bi} is independent of the electrically 'inactive' thickness in all instances it is evident that the measurement of the value of V_{bi} is around half the theoretically predicted value of 1.34 V. In this paper, we will show that a combination of effects such as the electrical damage of the specimen introduced during FIB milling (Brown *et al.*, 1999) and the effects of electron irradiation are responsible for this discrepancy (Houben *et al.*, 2005; Cooper *et al.*, 2007).

In situ annealing to reduce the electrically 'inactive' thickness

The presence of amorphous layers on semiconductor specimens that have been prepared in the FIB have been studied extensively but information on the electrical damage of these specimens is more scarce. It has been shown that when GaAs is exposed to low doses of 30 kV Ga ions ($<10^{13}$ cm^{-2}) the Fermi level at the specimen surface is pinned mid-gap even when the specimen retains its crystalline structure (Brown *et al.*, 1999). It has also been shown that annealing the specimens in the temperature range 200 to 600 °C can be used to remove electrical defects (Pons and Bourgoin, 1985).

The GaAs *p-n* junction specimen, 'A' described earlier, was annealed *in situ* in the TEM to temperatures of 200, 300, 400, 500 and 600 °C for 1 h, with a cooling period of 30 min between each elevated temperature. Holograms were acquired at each elevated temperature and to assess the improvement in the specimens, holograms were acquired at room temperature in-between each annealing step. The experimental conditions such as the hologram acquisition time and the intensity of the electron illumination were kept constant. The specimens were believed to have cooled to room temperature between each annealing stage as no specimen drift was observed.

Figure 5 shows phase images from a 240-nm-thick GaAs membrane containing a *p-n* junction acquired at room temperature, before the annealing and at room temperature after the 500 °C anneal stage. The improvement in the signal-to-noise ratio in the regions of the phase image that contain the specimen after annealing is clear.

Figure 6(a) shows profiles extracted from the reconstructed phase image across a 300-nm-thick GaAs membrane containing a *p-n* junction. The step-in phase across the junction before annealing is 0.7 radians, corresponding to a value of V_{bi} of 0.32 V. The step-in phase measured at room temperature after a 500 °C anneal has increased to 2.0 radians, corresponding to an V_{bi} of 0.91 ± 0.10 V. Although this is a considerable improvement it is still much smaller than expected from theory.

Figure 6(b) shows the effect of successive annealing and cooling on the measured step-in phase across the *p-n* junction. The horizontal axis shows the temperature at which each measurement was made. The low signal-to-noise ratio in the

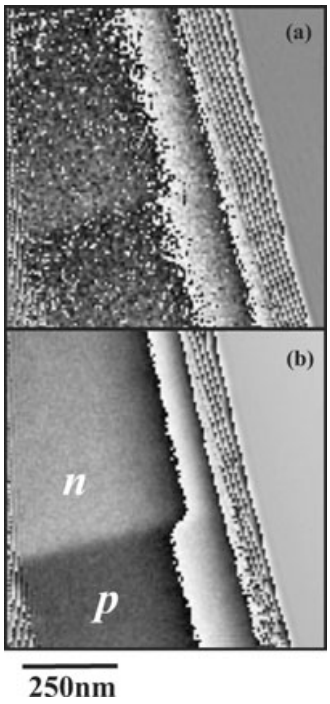

Fig. 5. Reconstructed phase image of a 240-nm-thick GaAs membrane containing a *p-n* junction acquired at (a) room temperature and (b) at room temperature after a 500 °C anneal. These phase images have not been unwrapped and the phase is displayed in multiples of 2π.

phase images recorded of the 360-nm-thick membrane did not permit the reconstruction of phase images acquired using a 4 s time period. To measure the phase across the junction at the start of the experiment and hence to assess the improvement in the step-in phase across the junction over the whole annealing experiment, a longer acquisition time was used to improve the signal-to-noise ratio in the phase image, but only for the first acquisition at room temperature before annealing. After a 400 °C anneal, the signal-to-noise ratio had improved such that the holograms could be recorded from this membrane using the 'standard' experimental acquisition time and reconstructed successfully.

A surprising result is that at elevated temperatures, the value of V_{bi} calculated directly from the phase increases linearly in the temperature range 200 to 400 °C, contrary to theoretical predictions. A possible explanation for this effect is that the intrinsic carrier density in the specimens is also reduced after FIB milling, leading to an extension of the extrinsic regime to higher temperatures (Sze, 2002). In addition, the step-in phase measured across the junctions at room temperature is reduced after an anneal of 600 °C, which is consistent with the changes in the structure of the specimen reported in the literature (Miyake *et al.*, 1988).

Figure 6(c) shows the step-in phase measured across the junctions, obtained from holograms acquired at room temperature before annealing and after the 500 °C annealing

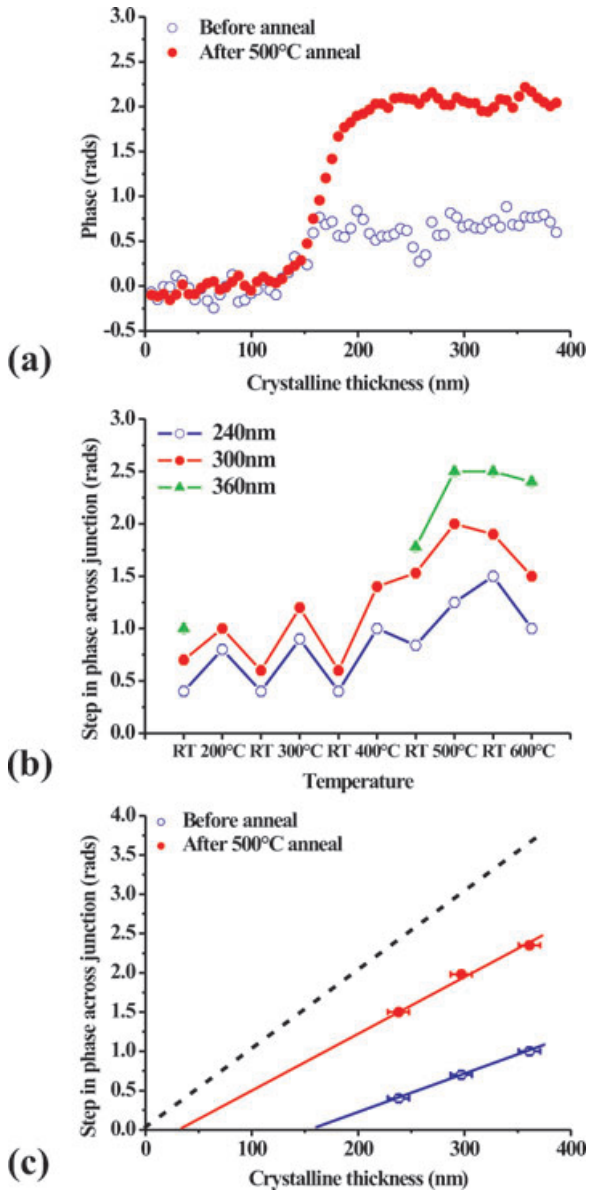

Fig. 6. (a) Step-in phase measured across a 300-nm-thick GaAs membrane containing a *p-n* junction at room temperature, and before and after a 500 °C anneal. (b) The effect of successive *in situ* annealing and cooling on the step in the measured phase shift across the junction. The horizontal axis shows the temperature, at which each measurement was made. RT indicates room temperature. (c) The step in phase plotted as a function of crystalline thickness measured before and after annealing at 500 °C. The theoretical bulk properties are indicated by the dashed line. The electrically 'inactive' thickness on each specimen surface has been reduced from 80 to 17 nm.

stage as a function of crystalline specimen thickness. The electrically 'inactive' thickness on each specimen surface measured using the *x*-intercept has been reduced from 80 to 17 nm which is a significant improvement. The presence of an electrically 'inactive' region after annealing could be due to the presence of complex defects that can not be removed during the annealing stage, and also from surface depletion.

By using the gradients in Fig. 6(c) to calculate a value for V_{bi}, an improvement from 0.67 ± 0.10 V to 1.00 ± 0.10 V after the annealing is observed, the theoretical value of 1.34 V is indicated by the dashed line. Clearly, the theoretical V_{bi} is not recovered and reasons for this discrepancy will be suggested later in this paper. Calculations of dopant diffusion distances suggest that the Si *p*-type dopants move over a distance of less than 1 nm after a 1 h 500 °C anneal, and 2 nm for the Be *n*-type dopants. These calculations suggest that dopant diffusion is not the principle mechanism behind the discrepancy between the theoretical and measured V_{bi}. However, these diffusion distances should be considered as lower limits as the dopants are expected to diffuse faster in highly faulted material, such as FIB-prepared TEM specimens (Fahey *et al.*, 1989).

In situ annealing has been used to provide a significant noise reduction in the phase images of the GaAs FIB-prepared *p-n* junctions as well as increasing the measured phase. These results suggest that annealing removes the defects resulting from both Ga implantation and the subsequent collisions in the lattice which has the effect of reactivating dopants in the specimens.

Annealing at 300 °C has also been used to improve the quality of FIB-prepared Si specimens reducing the electrically 'inactive' thickness on each surface from 25 to 5 nm (Cooper *et al.*, 2006).

The measurement of the built in potential in the *p-n* junctions using *in situ* electrical biasing

An alternative approach of measuring a value of V_{bi} using a method that is independent of both the amorphous and 'electrically' inactive thicknesses is to apply an electrical bias to the junction *in situ* in the TEM (Twitchett *et al.*, 2002). A value for V_{bi} can be determined by plotting the reverse bias voltage as a function of the step-in phase measured across the *p-n* junction using Eq. (5), where V_{app} is the applied reverse bias voltage and t_{active} is the electrically 'active' thickness, where $t_{active} = t_{crystalline} - t_{inactive}$. It is assumed that the electrically 'inactive' thickness on the specimen is constant during biasing.

$$\Delta\phi = C_E(V_{bi} + V_{app})t_{active} \quad (5)$$

To bias the *p-n* junction *in situ*, a new GaAs *p-n* junction was grown onto a lightly doped *p*-type conducting substrate. The specimens were prepared such that they could be biased in the TEM using a dedicated single-tilt two-contact holder (Twitchett *et al.*, 2002). The specimen was mechanically thinned to ~150 μm and sputtered with gold onto each surface to provide improved electrical contacts. The central section of the specimen was then selected by cleaving the outer regions from the specimen such that the junction was not electrically shorted by the gold coating. The *p-n* junction

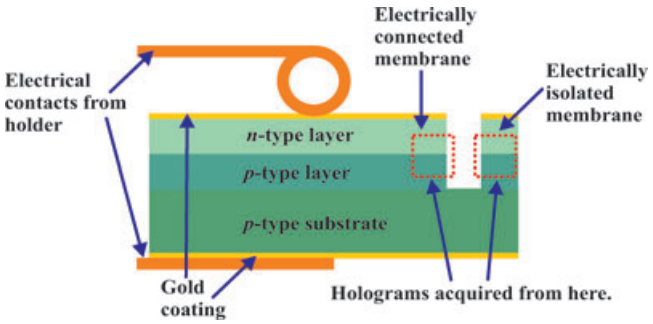

Fig. 7. Schematic diagram showing the specimen geometry used in the biasing experiments. The presence of an electrically connected and an electrically isolated membrane can be seen. The holograms were acquired from the regions indicated.

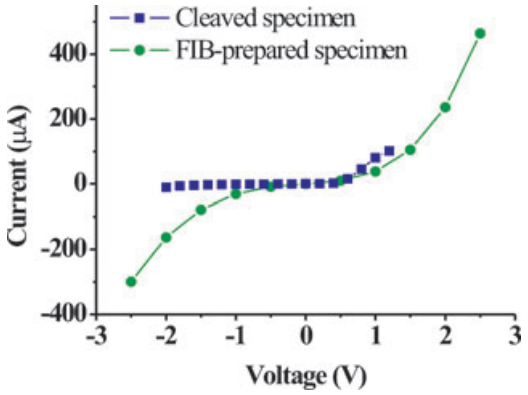

Fig. 8. Current-voltage characteristics for the cleaved and FIB-prepared GaAs *p-n* junction in the biasing holder.

was electrically tested in the biasing holder to ensure that the current–voltage behaviour of the system was consistent with theory. For the initial testing, the specimen was only biased in the range 1.2 to −2.0 V to avoid damaging the junction before TEM examination. The specimen was then FIB-milled such that a thin membrane suitable for examination by electron holography was situated close to a region of vacuum. Figure 7 shows the geometry used. A vacuum cut was made to create an electrically connected and an electrically isolated membrane of identical thickness.

Holograms of the membranes were acquired before biasing in order to record the phase shift across the junction directly after FIB-milling. The current-voltage characteristics of the system were then re-tested. The phase shift measured across the FIB-prepared junction, measured before and after electrical tests were identical, suggesting that applying a bias voltage to the specimen does not appear to re-activate the dopant atoms in the junction.

Figure 8 shows the change of the electrical properties of the *p-n* junction both before and after FIB-milling. The cleaved specimen behaves as a diode, allowing current to flow at forward bias and preventing flow at reverse bias. After FIB

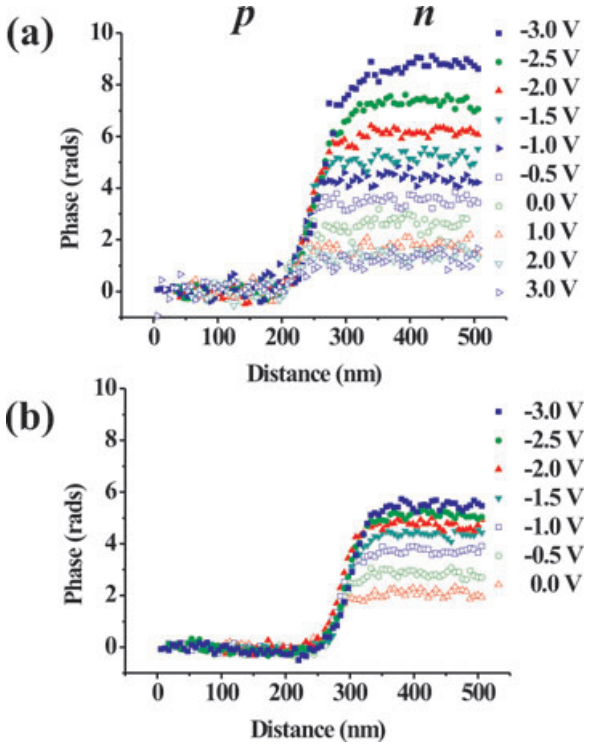

Fig. 9. Phase profiles across the GaAs *p-n* junction in the (a) electrically connected membrane and the (b) electrically isolated membrane.

milling, the specimen allows current flow in both directions indicating that the electrical properties of the junction have been modified by the specimen preparation.

The results of the biasing experiment are shown in Fig. 9 where (a) shows the phase measured across the electrically connected junction and (b), the electrically isolated junction. As expected, both the value of the V_{bi} and the depletion width increase as a function of applied reverse bias for the electrically connected junction. However the electrically isolated membrane is also biased possibly due to the fact that the *p-n* junction does not extend across the whole thickness of the specimen and that the damaged surface layers can provide a conduction path across the junctions.

Figure 10 shows the step in phase measured across the electrically 'connected' *p-n* junction as a function of applied reverse bias. At reverse bias voltages greater than −3.0 V, the effects of breakdown are apparent; therefore, the gradient is plotted only in the voltage range 0.0 to −3.0 V. From the gradient the electrically 'active' thickness can be determined and here it is found to be 241 ± 10 nm, which from equation (5), corresponds to a V_{bi} of 1.36 ± 0.05 V. The crystalline thickness of the specimen measured using CBED is 430 ± 10 nm. Therefore the electrically 'inactive' thickness of the specimen is approximately 190 nm, consistent with the other specimens prepared using 30 kV Ga ions in the FIB.

The value of V_{bi} calculated by applying a reverse bias across the specimen is consistent with the theoretical value of

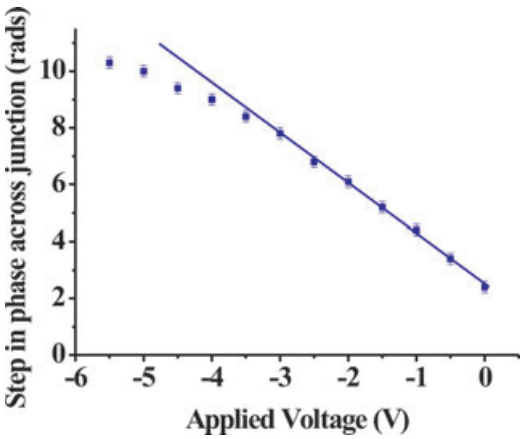

Fig. 10. Step-in phase across the GaAs *p-n* junction as a function of applied reverse bias. A gradient is plotted only in the voltage range 0.0 to −3.0 V, because the effects of reverse breakdown would affect the results.

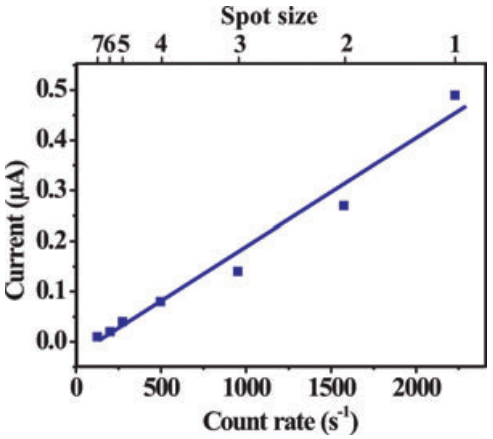

Fig. 11. The current measured from the *p-n* junction mounted in the *in situ* biasing holder as a function of both spot size and incident electron beam intensity.

1.34 V. Two different specimens were prepared from the same wafer and evaluated and multiple data sets were obtained, giving V_{bi} in the range 1.25 to 1.40 V. The poor signal-to-noise ratio in the phase images of the GaAs *p-n* junctions, especially at low reverse bias voltages, explains the relatively large range of the value of V_{bi} that was measured. The signal-to-noise could be improved by annealing the specimen, although incompatibility between the *in situ* annealing and biasing holders have prevented the successful biasing of an annealed specimen. Attempts to anneal specimens in vacuum ovens have also proved unsuccessful up to this time due to the quality of the vacuum. It has also been shown that by using the latest generation of electron microscopes with excellent stability, holograms can be acquired for time periods of more than 1 min using very low electron beam intensities, which lead to reconstructed phase images with excellent signal-to-noise ratios (Cooper *et al.*, 2007).

So why is the theoretical V_{bi} recovered when using an applied reverse bias across the *p-n* junction compared to when the phase is evaluated as a function of specimen thickness? Both approaches are in principle independent of the electrically 'inactive' thickness.

During the *in situ* biasing experiments, it was observed that a conduction current was present through the *p-n* junction even with no bias voltage applied. Figure 11(a) shows the current measured as a function of both the spot size of the electron beam and the intensity of the electron beam. The electron intensity was controlled by reducing the spot size whilst maintaining a constant area of illumination on the specimen (the setting of the first condenser lens, known as the spot size, determines the flux of electrons collected by the aperture before the second condenser lens). The current measured is clearly dependent on the intensity of the electron radiation. The electron intensity is indicated as the mean number of electrons recorded on each CCD pixel per second.

During TEM examination, electron-hole pairs are generated in semiconductor specimens, particularly in GaAs as it is a direct bandgap semiconductor (Williams & Carter, 1996). In a *p-n* junction, the electric field will cause the electrons and holes to separate, with the holes drifting towards the *n*-doped regions and the electrons towards the *p*-doped regions. When using a biasing holder, these excess carriers are removed from the region of interest; however, when examining specimens using conventional preparation techniques, the build-up of these carriers will influence the phase measured across the junctions.

To assess the reasons behind the discrepancy between V_{bi} measured using each of the different experimental methods described, the GaAs *p-n* junctions were examined to assess the effect of the specimen–electron beam interactions on the measured phases.

The effects of specimen charging in the TEM

The GaAs specimen grown on the conducting substrate was prepared in the FIB using conventional 'trench' geometry and examined using the same procedure as described previously. Figure 12 shows the step-in phase measured across all of the *p-n* junctions as a function of crystalline specimen thickness measured using CBED. The value of V_{bi} for the specimens grown onto the non-conducting substrate was previously measured to be approximately 0.7 V. Using the gradient shown in Fig. 12, the V_{bi} for the specimen with a conducting substrate is 0.96 ± 0.10 V. The 228 ± 15 nm electrically 'inactive' thickness measured from the *x*-intercept is slightly higher than observed in the specimens with the undoped substrate. Possible reasons for this discrepancy could be due to small differences in the FIB milling procedure. For comparison, the step in phase measured across the *p-n* junctions examined in the biasing holder at zero bias is shown.

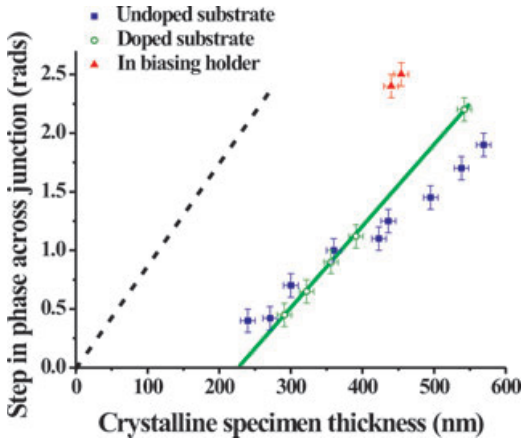

Fig. 12. The step in phase measured across the *p-n* junctions as a function of the crystalline specimen thickness measured using CBED. Specimens that have good conduction paths to earth exhibit a larger V_{bi} across the junction than the specimens with poor conduction paths. For the specimens with the conducting substrate, a value of V_{bi} of 0.96 ± 0.10 V is calculated from the gradient, whereas for an identical specimen with an insulating substrate the value is only 0.70 ± 0.10 V. The values that would be expected theoretically from a bulk-like specimen are shown using a dashed line.

For the specimens that have the best conduction paths to earth, the largest value of V_{bi} is measured across the junction.When compared, the value of V_{bi} measured for the specimens grown with a conducting substrate is larger than those with the non-conducting substrate. In comparison, the specimens mounted in the biasing holder exhibit almost twice the step-in phase per unit thickness compared to those specimens with a non-conducting substrate.

The effects of the electron beam on the measured step-in phase across a *p-n* junction were assessed by varying the beam intensity using the same method as described earlier, i.e. by adjusting the spot size of the beam while keeping the area of the illumination constant. To remove artifacts from a slight thickness variation across the specimen, the phase profiles have been flattened using the *p*-side of the junction. Figure 13(a) shows the phase measured across a *p-n* junction grown onto a conducting substrate as a function of spot size. There is a clear trend showing a reduction in the measured phase as the intensity of the electron beam is increased.

It is known that the build up of charge can be reduced by carbon coating the specimen on one side (McCartney *et al.* 2002). Figure 13(b) shows the phase measured across the junction after carbon coating as a function of the intensity of the electron irradiation. Although a significant improvement is observed, the electron beam still influences the measurement. Figure 13(c) shows the effect of varying the strength of the electron beam on the phase for a GaAs *p-n* junction examined in the *in situ* biasing holder. The specimen in the biasing holder has not been carbon coated. The difficulty in forming good quality holograms when using an intense

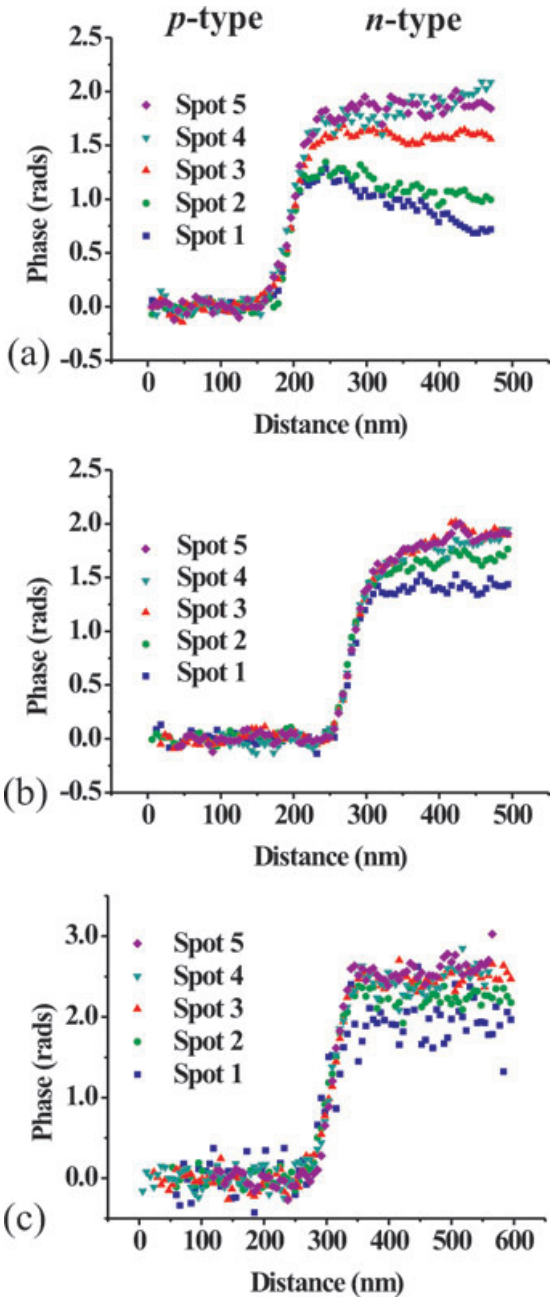

Fig. 13. (a) The phase measured across a *p-n* junction with a doped substrate using different electron beam intensities. (b) As (a) except after coating the specimen with 20 nm carbon on one side. (c) The phase measured across a *p-n* junction examined in the biasing holder using different electron beam intensities. The poor signal-to-noise ratio for the phase measured using spot 1 reflects the difficulty in performing holography using an intense electron beam with lower coherence. The presence of the electrical connections to the biasing holder can also interfere with the formation of electron holograms when they are disturbed by small movements of air in the room.

electron beam is reflected in Fig. 13(c) where the signal-to-noise ratio at spot size 1 is very poor. However it can be observed that, with the exception of the strongest electron beams, the phase profiles measured across the junction are identical for the different electron beam intensities used.

Figures 13(a) and (b) also show that the phase profiles are asymmetric, even from the phase images reconstructed using the low-intensity electron beams. These profiles suggest that the build-up of charge in the specimens affects the *n*-side of the junction more than the *p*-side. This is probably due to the fact that the *n*-doped region on the surface layer on the specimen is electrically isolated from the substrate by the presence of the junction, which leads to a build-up of trapped charge in this region (although, as has been shown, some charge may be removed by the presence of the electrically 'inactive' thickness). Figure 13(c) shows that when electrical connections are applied to the specimen, the profiles are more symmetrical, reflecting the actual dopant distribution in the specimen.

Values of V_{bi} were determined experimentally using the approaches described previously except using different intensity electron beams to form the holograms (Spot sizes 2 and 4). Figure 14(a) shows the step-in phase measured across a carbon coated specimen as a function of crystalline specimen thickness measured using CBED. The holograms formed using spot 2 are approximately five times more intense than for spot 4.

The values of V_{bi}, determined directly from the gradients are 0.95 V using spot 4 and 0.85 V using spot 2, demonstrating that the intensity of the electron irradiation influences the determination of V_{bi} even after carbon coating. Figure 14(b) shows the step-in phase measured across the junction as a function of applied reverse bias examined using the *in situ* biasing holder at spots 2 and 4. The value of V_{bi} measured using this approach is unchanged for each spot size used, and as shown previously, consistent with theory.

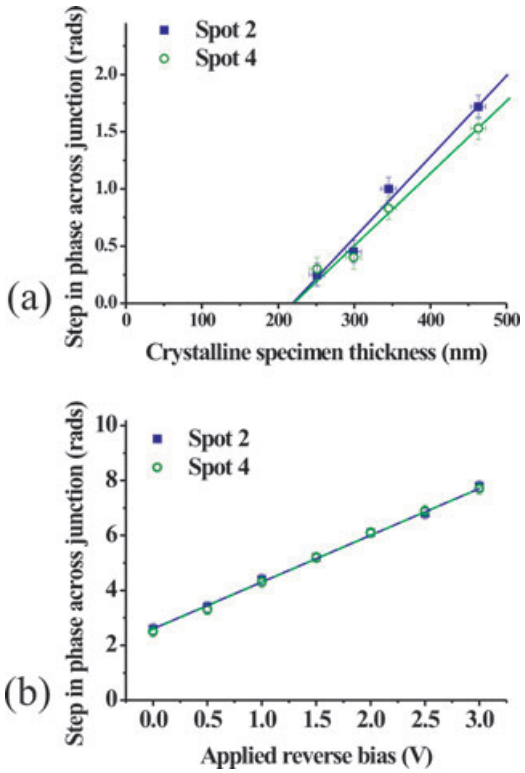

Fig. 14. (a) Step-in phase, plotted as a function of crystalline specimen thickness across a carbon-coated FIB-prepared GaAs *p-n* junction on a doped substrate measured using spot sizes 2 and 4 for a constant area of illumination. The values of V_{bi} determined from the gradients are 0.85 and 0.95 ± 0.10 V for spot sizes 2 and 4, respectively. (b) Step-in phase measured across a 440-nm-thick GaAs *p-n* junction on a doped substrate, plotted as a function of applied reverse bias voltage for spot sizes 2 and 4 and for a constant area of illumination. For each spot size the value of V_{bi} is calculated as 1.36 ± 0.05.

Reducing the effects of specimen charging by using metal coatings

In order to reduce the build up of charge in the regions of interest and improve the specimens for electron holography, a specimen was prepared from the wafer with the conducting substrate using a FIB operated at 30 kV. However, before the final milling stage the specimen was removed from the FIB and sputter coated with a few tens of nanometres of platinum. The specimen was then finished using the FIB to remove the platinum from only the regions of interest.

Figure 15(a) shows a SEM image of the specimen, the regions of the membranes that are coated in platinum are shaded. Figure 15(b) shows the step-in phase measured across the *p-n* junctions as a function of the crystalline specimen thickness measured using CBED for the specimens coated in platinum, for the specimens prepared using the standard procedure and for the specimens examined in the biasing holder. It is clear that a higher step-in phase is measured across the junctions that have been coated in platinum compared to those with no coating. By using this method, a value for V_{bi} of 1.26 ± 0.10 V is measured, which is just within the margins of experimental error. This is significantly higher than the 0.96 V that is measured when no platinum coating is used. As demonstrated previously, the electrically 'inactive' thickness does not appear to be affected by the charging of the specimens. In addition, the platinum coating does not appear to be as effective as using electrical contacts that are applied directly onto the specimen such as in an *in situ* biasing holder for removing charge from the specimens.

Reduction of the electrically 'inactive' thickness using low energy FIB milling

The results from the annealing experiment have indicated that one of the principle mechanisms that cause the electrically

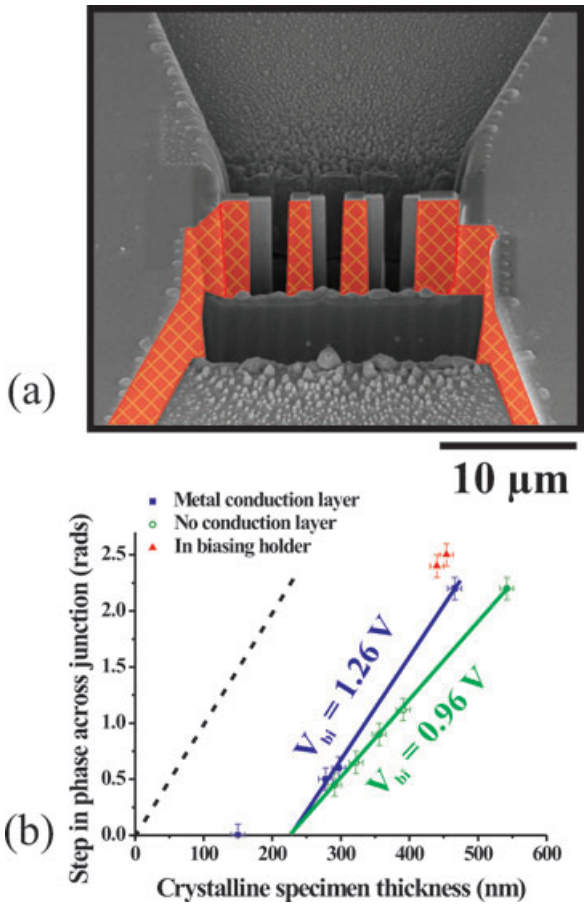

Fig. 15. (a) Scanning electron image of the specimen. The regions on the membranes that remain coated in platinum after the specimen is finished are shaded. (b) Step-in phase measured across the *p-n* junctions as a function of crystalline specimen thickness for the membranes. For comparison, data is shown for specimens without the platinum coating and for specimens examined in an *in situ* biasing holder. Values of V_{bi} of 1.26 and 0.96 ± 0.10 V are measured from the gradient for specimens with and without metal coating, respectively. The values that would be expected theoretically from a bulk like specimen are shown using a dashed line.

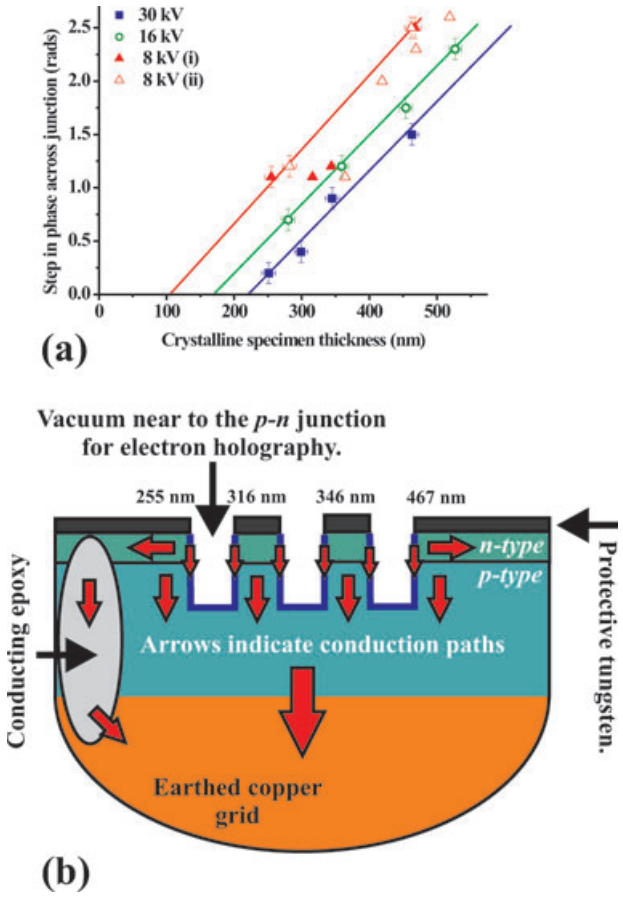

Fig. 16. (a) Step-in phase measured across the *p-n* junctions as a function of crystalline specimen thickness measured using CBED. Only the data points shown with error bars, representing the membranes positioned at either side of the specimen have been used to calculate the gradients. A second specimen (ii) was prepared using 8 kV Ga ions in order to provide more data points. The electrically 'inactive' thicknesses are 223, 172 and 100 ± 15 nm for the specimens prepared using 30, 16 and 8 kV Ga ions, respectively. (b) A schematic of the specimen prepared using 8 kV Ga ions showing the different thickness membranes and indicating the possible conduction paths to earth for the carriers generated in the *p-n* junctions.

'inactive' thickness are defects in the specimen that are introduced during FIB-preparation. It has been shown that by lowering the operating voltage of the FIB the thickness of the amorphous layer on the specimens can be reduced (Kato *et al.*, 1999). Simulations suggest that the range of the incident Ga ions are reduced at lower energy (Ziegler, 2004), which may, as a consequence, result in a reduction in the thickness of the electrically 'inactive' layer.

Specimens were prepared using conventional 'trench' geometries for examination using FIB-operating voltages of 30, 16 and 8 kV. For each operating voltage, membranes with different thicknesses were prepared such that the step in phase across the junctions could be investigated as a function of crystalline specimen thickness. Electron holograms were acquired using the same procedure as described in previous sections.

Figure 16(a) shows the step in phase measured across the *p-n* junctions as a function of crystalline specimen thickness measured using CBED. The relationship between the phase and the specimen thickness for the specimens prepared using operating voltages of 30 and 16 kV is approximately linear. However, for the specimens prepared using the FIB operated at 8 kV the relationship is more complex.

Figure 16(b) shows a schematic of a FIB-prepared specimen containing a *p-n* junction indicating the conduction paths that are available for the electrons and holes that are generated in the specimens to be conducted to earth. For the membranes located at either side of the specimen there is a conduction path

Table 2. V_{bi} and $t_{inactive}$ measured for the GaAs *p-n* junctions prepared using different FIB operating voltages.

Specimen	V_{bi}/V	$t_{inactive}$/nm
30 kV	0.93 ± 0.10	223 ± 15
16 kV	0.88 ± 0.10	172 ± 15
8 kV	0.94 ± 0.10	100 ± 15

away from the region of interest whereas for the membranes in the central regions of the specimen the charge can only be removed by the damaged surface regions of the specimens. It is possible that for the specimens prepared using 8 kV ions the reduced surface damage is not as effective at removing the carriers generated in the specimen, hence the reduction in the step in phase measured across the junctions that are positioned in the centre of the specimen which are electrically isolated. For this reason, only the data acquired from the sides of the specimen have been used to plot the gradient. As it is undesirable to use only two data points to plot a gradient, a second specimen, indicated as (ii), was prepared and examined using an identical procedure.

Table 2 shows the calculated values of V_{bi} and $t_{inactive}$ for each specimen. It can be seen that the electrically 'inactive' thickness is systematically reduced from 220, 172 and 100 ± 15 nm for specimens prepared using FIB-operating voltages of 30, 16 and 8 kV, respectively.

The values of V_{bi} remain roughly constant for each of the specimens to within experimental error and are also consistent with those measured previously.

As expected, the electrically inactive layer has been reduced by lowering the operating voltage of the FIB. By using Ga ions with less energy, the thickness of the modified regions on the specimens surfaces is reduced. However, the reduction of the electrically 'inactive' thickness for some specimen geometries can also reduce the conduction path to earth that can remove *some* of the build-up of charge in the specimens.

Discussion

Electron holography can be used to quantitatively measure the dopant concentration in FIB-prepared GaAs *p-n* junctions. The discrepancies between the theoretical and measured potentials in *p-n* junctions are due to three principle mechanisms, the creation of electronic states mid-bandgap due to the presence of defects, from specimen charging during examination and a contribution from the effects of band bending near the specimen surfaces (Sze, 2002) that have not been systematically investigated here.

Defects created in the FIB-prepared GaAs *p-n* junctions have the effect of pinning the Fermi level resulting in a reduction of the electrical potential measured across the junctions. It has been shown that low temperature annealing removes many of these defects which are the principal causes of the electrically 'inactive' thickness. The reduction of the electrically 'inactive' thickness has the effect of increasing the phase measured across the junctions which leads to an improvement of the signal-to-noise ratio. The electrically 'inactive' thickness can also be reduced by operating the FIB at lower voltages.

Two different approaches have been used to measure a value of V_{bi} that are both, in principle, independent of the electrically 'inactive' thickness. By plotting the step-in phase across the junctions as a function of the crystalline specimen thickness, V_{bi} is found to be much less than predicted by theory, even after annealing the specimens. By attaching electrical contacts and measuring the step-in phase as a function of reverse bias applied *in situ*, the correct value of V_{bi} was recovered. The experimental evidence suggests that for GaAs *p-n* junctions, the build-up of charge is responsible for the reduction of the potential in the junctions and that the presence of good quality connections can remove this charge and allow the recovery of the predicted value of V_{bi}.

After annealing, the electrically 'inactive' thickness was still 17 nm on each surface and the theoretical value of V_{bi} was not recovered. Further investigation is required to assess whether these discrepancies are partly due to the effects of surface band bending as well as from damage in the specimen that was not repaired during the annealing.

By biasing the specimen *in situ*, the electrically 'active' thickness can be determined leading to a measurement of V_{bi}. To improve this measurement the specimens could be annealed or prepared using a low energy Ga ion beam to reduce the electrically 'inactive' thickness and improve the signal-to-noise ratio. Although the application of electrical contacts to simple *p-n* junctions is straightforward, the task appears somewhat more formidable for the characterization of nano-scale devices. However, the experimental results suggest that *in situ* biasing is necessary for direct quantitative characterisation of the *p-n* junctions examined here.

Conclusion

Specimen preparation and the interaction between the electron beam and the specimen have significant effects on the phase measured using electron holography and the utmost care should be taken when using electron holography to measure the dopant concentration in all semiconductor materials. Fortunately, the measurements of the potentials do appear to be reproducible when using carefully defined specimen preparation techniques and microscope operating parameters. By using the latest generation of microscopes which exhibit excellent stability we hope to be able to improve the accuracy of our measurements of the phase in semiconductor specimens (Cooper *et al.*, 2007) and ultimately be able to accurately interpret these measurements in terms of carrier concentrations.

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