Off-axis electron holography of focused ion beam milled transistors

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Summary: The use of off-axis electron holography to study transistors prepared for TEM examination using focused ion beam milling is presented. Methods for removing artifacts caused by sample thickness variations and charging are outlined.

1. Introduction

Rau et al. (1999) recently used off-axis electron holography in the transmission electron microscope (TEM) to form two-dimensional maps of the electrostatic potential in transistors that had been thinned using mechanical polishing and ion milling [1]. *n*- and *p*-type regions were distinguished readily as bright and dark contrast in phase images, respectively. Here, we discuss the application of electron holography [2] to transistors prepared using focused ion beam milling (FIB), a technique that is now widely used to prepare TEM samples in the semiconductor industry.

2. Experimental

Samples were prepared for TEM examination using FIB (Fig. 1).Off-axis electron holograms were recorded at 200 kV in a Philips CM200 FEG (field emission gun) TEM and at 300 kV in a JEOL 3000F FEG TEM. Similar results were obtained from samples of two different thicknesses using both microscopes.

3. Results and Discussion

a) Focused ion beam milling of a wafer that has a range of compositions on its top surface results in thickness corrugations in the doped region beneath (Fig. 1). Fig. 2a shows an electron hologram of part of the PMOS transistor labelled D in Fig. 1. Rapid thickness variations can be seen in the Si substrate, both in the amplitude and particularly in the phase of the reconstructed image wave (Figs. 2b and 2c, respectively). One solution is to determine this (1-D) thickness variation from the region far below the source and drain of the transistor and then to remove the 'corrugation' from the entire sample to leave the depletion region potential of interest (Fig. 2d). An alternative solution is to perform the final milling from the substrate side (Fig. 3). Milling from several directions also allows the very surface of the wafer to be removed, reducing the size of the overlap needed in the hologram between vacuum and the doped region.

b) The majority of semiconductors examined using holography exhibit some form of charging in the TEM, which is often only visible in the reconstructed phase image. Before acquiring the images shown in Fig. 2, the sample was thus coated with a few nm of carbon. Without carbon, the reconstructed phase image took the form shown in Fig. 4a. The rapid variation in phase, which results from charging, would have precluded mapping of the depletion region potential.

c) Rau et al. (1999) pointed out that surface depletion creates an electrically 'dead' layer on the top and bottom surface of a doped sample. They found that the thickness of this layer was ~25 nm on each of the two surfaces. A similar analysis yielded a value of ~50 nm for the sample shown in Fig. 2, which has a total thickness of ~340 nm. This large value explains why a sample that had a total thickness of ~100 nm was found to show no dopant contrast (Fig. 4b).

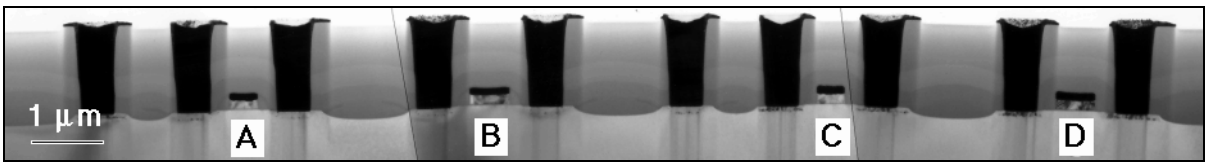

Figure 1: *Transistor sample prepared by FIB. A, B, C and D are NMOS (0.35µm gate), NMOS (0.5µm gate), PMOS (O.35µm gate) and PMOS (0.5µm gate) transistors, respectively.*

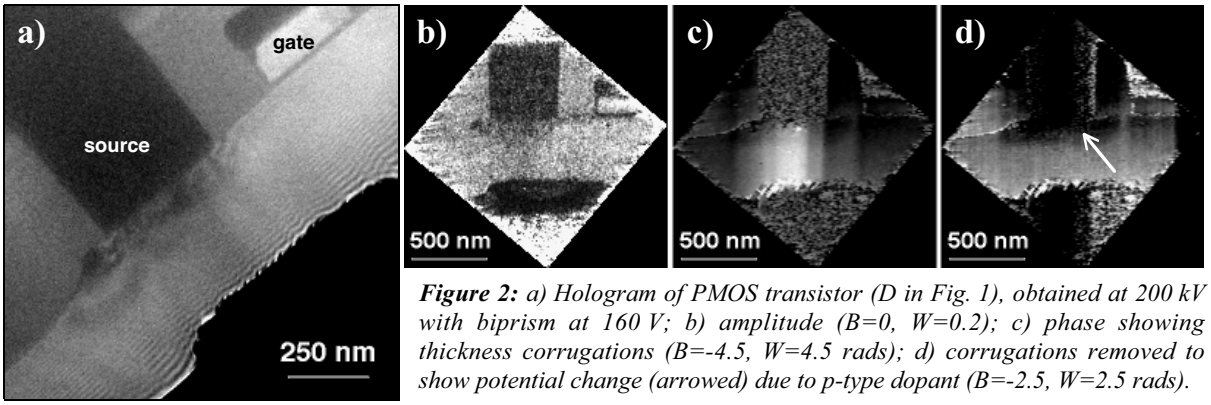

Figure 2: *a) Hologram of PMOS transistor (D in Fig. 1), obtained at 200 kV with biprism at 160 V; b) amplitude (B=0, W=0.2); c) phase showing thickness corrugations (B=-4.5, W=4.5 rads); d) corrugations removed to show potential change (arrowed) due to p-type dopant (B=-2.5, W=2.5 rads).*

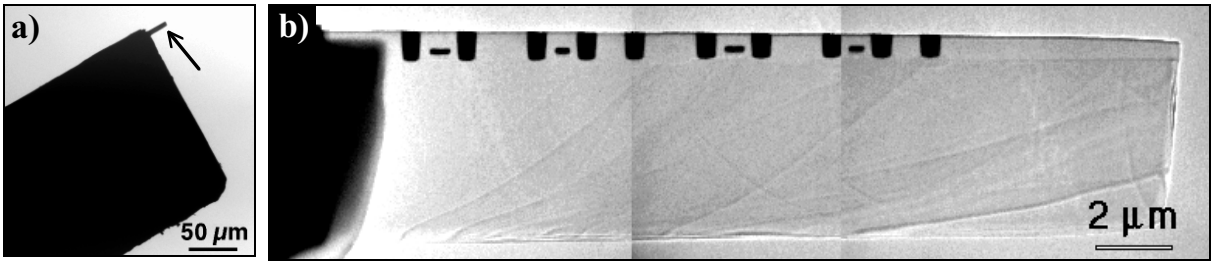

Figure 3: *Bright field images of sample milled in several directions using FIB (final thinning from substrate side), with surface subsequently cleaned using low angle ion milling in a Gatan PIPS. Membrane is arrowed in a).*

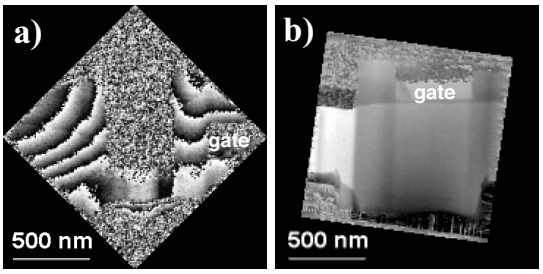

Figure 4: ***(****Wrapped) phase images of identical transistor to that shown in Fig. 2, both obtained at 200 kV with a biprism voltage of 140 V. a) Sample of thickness 340 nm, examined* ***before depositing*** *carbon onto it to prevent charging; b) Sample of thickness 100 nm. No contrast is visible at the position of the p-type dopant because the combined thickness of the surface depletion layers at the top and bottom surfaces of the sample is comparable to the total sample thickness.*

4. Conclusions

Off-axis electron holography has been used to examine dopant contrast in transistors prepared for TEM examination using FIB. Artifacts associated with sample thickness variations and charging have been identified, and methods for removing them have been proposed. It should be noted that future work is still required to understand the physics that relates electrostatic potentials measured in semiconductors in the TEM to the forms of the conduction and valence bands.

References

[1] W. D. Rau et al., Phys. Rev. Lett. **82** (1999) 2614.
[2] R. E. Dunin-Borkowski et al., Recent Res. Devel. in Applied Phys. **1** (1998) 119.