Ge/GeSn Quantum Well MOSFETs for Cryogenic Applications

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***Abstract*— Cryogenic CMOS provides critical performance benefits for high-performance computing, space electronics, and quantum interfaces due to enhanced carrier mobility and steeper subthreshold swing (SS). However, the band-tail effect limits the device performance at cryogenic temperatures. In this work, Ge/GeSn quantum well (QW) p-MOSFETs are studied from 300 K down to 5 K. Owing to the QW confinement and the presence of a Ge cap layer, interface-related band-tail states are significantly suppressed. As a result, the Ge/$Ge_{0.88}Sn_{0.12}$ QW device exhibits a continuously decreasing SS, reaching 15 mV/dec at 5 K, which is the lowest reported SS among the Ge-based p-MOSFETs. This work highlights GeSn QW engineering as an effective strategy for cryogenic CMOS applications.**

***Index Terms*— Cryogenic CMOS, GeSn, quantum well, subthreshold swing, band-tail states.**

I. Introduction

THE growing demand for high-performance computing (HPC) driven by artificial intelligence (AI) and deep learning poses severe power challenges for advanced CMOS technologies [1]. Cryogenic CMOS (Cryo-CMOS) offers a promising solution [2]. At cryogenic temperatures (Cryo-T), reduced phonon scattering enhances carrier mobility, while a lower subthreshold swing (SS) enables voltage and power scaling [3]. However, conventional CMOS devices fail to fully exploit these intrinsic advantages because band-tail effects become pronounced at Cryo-T [4], [5]. As a result, SS saturates, the inflection phenomenon emerges, carrier mobility degrades, and low-frequency noise increases [6], [7], [8], [9], [10]. Facing these challenges, several approaches have been proposed to mitigate band-tail effects, including interface engineering or source/drain engineering through ion implantation into silicide process [11], [12], [13]. These strategies primarily suppress localized defects and interface traps induced band-tail states.

Ge(Sn)-based devices have emerged as highly promising candidates for cryogenic photonic [14], [15] and electronic applications [16], [17], [18], providing a material platform for seamless monolithic integration on a single chip. From an electronic perspective, their high carrier mobility enables high-frequency operation [17], [19], [20]. Moreover, the narrow bandgap of GeSn provides enhanced threshold voltage (V_{th}) tunability, effectively mitigating the critical challenge of V_{th} increase in Cryo-CMOS [4]. These unique attributes position GeSn devices as ideal candidates for high-performance, energy-efficient cryogenic applications [21].

In this work, we adopt a Ge/GeSn quantum well (QW) architecture to reduce band-tail-related transport degradation. The GeSn channel is spatially separated from the gate dielectric by a thin Ge interlayer, which suppresses wavefunction overlap with the dielectric interface, thereby mitigating Coulomb scattering, charge trapping, and mobility degradation caused by interface-localized states.

II. Device Fabrication

GeSn QW MOSFETs were fabricated on two different epitaxially grown heterostructures: a 4 nm Ge/6 nm $Ge_{0.96}Sn_{0.04}$/560 nm Ge/Si (100) and a 4 nm Ge/24 nm $Ge_{0.88}Sn_{0.12}$/580 nm Ge/Si (100). A device sketch is shown in Fig. 1(a). Figure 1(b) shows a cross-sectional TEM micrograph of the Ge/$Ge_{0.88}Sn_{0.12}$/Ge device, revealing a well-defined layer stack and a uniform HfO_2/Ge interface. The inset shows a high-resolution TEM image of the $Ge_{0.88}Sn_{0.12}$ channel layer with well-resolved lattice fringes, indicating good crystalline

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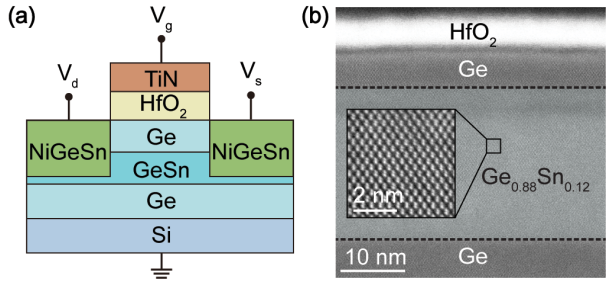

Fig. 1. (a) Schematic cross-sectional view of the GeSn QW pMOSFET. (b) Cross-sectional TEM image of the HfO_2/Ge/$Ge_{0.88}Sn_{0.12}$/Ge layer stack. The inset shows a high-resolution TEM image of the $Ge_{0.88}Sn_{0.12}$ layer.

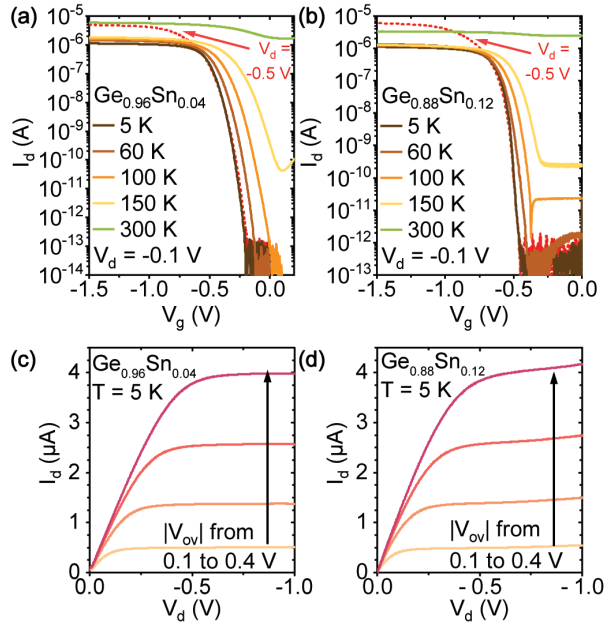

Fig. 2. Measured temperature-dependent transfer characteristics for Ge/GeSn QW devices with (a) $Ge_{0.96}Sn_{0.04}$ and (b) $Ge_{0.88}Sn_{0.12}$ wells at V_d = −0.1 V, with the dashed red curves at V_d = −0.5 V and 5 K. Output characteristics for the corresponding devices (c, d) measured at 5 K for gate overdrive voltages ranging from 0.1 to 0.4 V.

quality. A 6 nm $Ge_{0.96}Sn_{0.04}$/560 nm Ge layer with the same device dimensions was fabricated for reference without a Ge cap layer. The gate length and width are 15 μm and 60 μm, respectively. No intentional channel doping was introduced in any of the devices. The gate dielectric consists of 1 nm of Al_2O_3 deposited by atomic layer deposition (ALD) followed by O_2 plasma oxidation to form a thin GeO_x or $GeSnO_x$ layer and the deposition of 5 nm HfO_2 by ALD [17]. The metal gate consists of 45 nm sputtered TiN layer. The gate and mesa definition was performed by standard maskless lithography and reactive ion etching, followed by the deposition of Al_2O_3 as a passivation layer. Source and drain contacts were NiGeSn layers formed by annealing of a very thin Ni layer at 325 °C in forming gas for 10 seconds [22], [23].

III. Results and Discussion

The temperature-dependent electrical characteristics down to 5 K of the $Ge_{0.96}Sn_{0.04}$ and $Ge_{0.88}Sn_{0.12}$ QW devices are shown in Figs. 2(a) and (b). The transfer characteristics measured at a fixed drain bias (V_d) of −0.1 V exhibit a

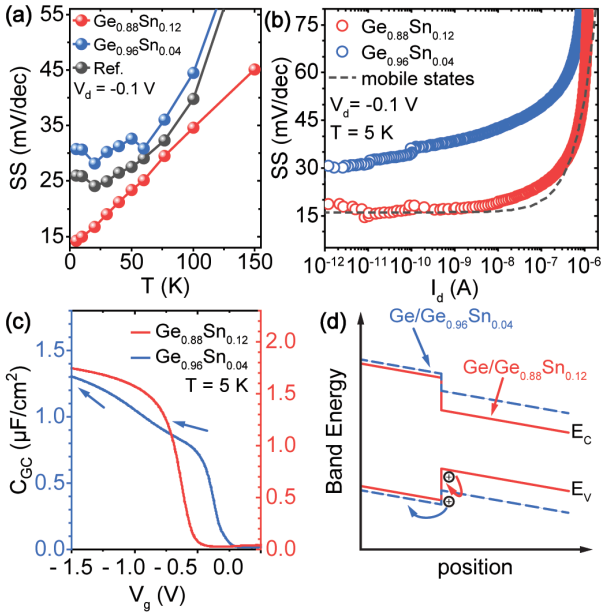

Fig. 3. (a) SS derived from measured I_d-V_g curves as a function of temperature for reference (black), $Ge_{0.96}Sn_{0.04}$QW (blue) and $Ge_{0.88}Sn_{0.12}$ QW (red) devices at V_d = −0.1 V. (b) SS-I_d characteristics extracted from measured I_d-V_g curves at 5 K and V_d = −0.1 V for $Ge_{0.96}Sn_{0.04}$QW (blue) and $Ge_{0.88}Sn_{0.12}$ QW (red); the dashed line denotes the calculated mobile-state limit. (c) Measured gate-to-channel capacitance versus gate voltage (C_{GC}-V_g) characteristics at 5 K for both devices. (d) Schematic band profiles of $Ge_{0.96}Sn_{0.04}$ QW and $Ge_{0.88}Sn_{0.12}$ QW devices.

reduction in the off-state current with decreasing temperature for both devices, consistent with bandgap increase and the suppression of thermally activated transport [21]. The on-/off-current ratio (I_{ON}/I_{OFF}) increases with decreasing temperature, exceeding 10^6 at 5 K. The transfer characteristics at V_d = −0.1 V and −0.5 V measured at 5 K show negligible threshold voltage shift and no SS degradation for both devices. The output characteristics measured for different overdrive voltages (V_{ov} = V_g - V_{th}) show well-defined linear and saturation regions as exemplified in Figs. 2(c) and (d), owing to the low Schottky barrier height of the NiGeSn/GeSn contacts (<0.06 eV for $Ge_{0.9}Sn_{0.1}$ [24]).

The temperature dependence of the SS for reference, $Ge_{0.96}Sn_{0.04}$ QW and $Ge_{0.88}Sn_{0.12}$ QW devices is shown in Fig. 3. Over the entire measured temperature range, the $Ge_{0.88}Sn_{0.12}$ QW device consistently exhibits the lowest SS. Correspondingly, the $Ge_{0.96}Sn_{0.04}$ QW and reference devices show stronger band-tail effects with a clear tendency toward SS saturation below ~50 K. Notably, the $Ge_{0.96}Sn_{0.04}$ QW device shows even more pronounced SS degradation than the reference device, indicating that a weak QW confinement alone is insufficient to reduce band-tail effects at low Sn content. In contrast, the SS of the $Ge_{0.88}Sn_{0.12}$ QW device continues to decrease with temperature, without signs of saturation. Linear fitting yields a slope of 0.216 mV/(dec·K) from 5 K to 150 K. At 5 K, a minimum SS of 15 mV/dec is obtained. Figure 3(b) shows SS-I_d characteristics for both QW devices at 5 K, and the dashed line represents the SS-I_d characteristic considering only mobile states, calculated following the model in Ref [5], [6], [7], [25]. The SS of $Ge_{0.96}Sn_{0.04}$QW device increases with I_d, showing a clear

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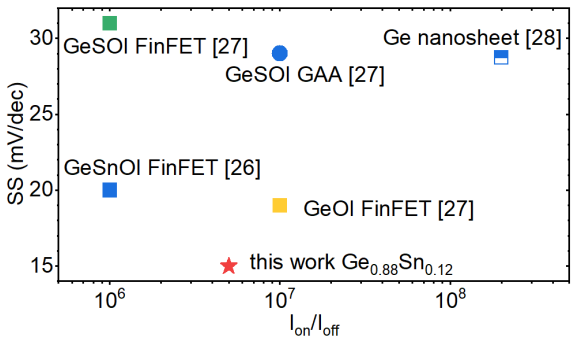

Fig. 4. Benchmarking of minimum SS versus I_{on}/I_{off} ratio at cryogenic temperatures for state-of-the-art Ge-based p-MOSFETs. The $Ge_{0.88}Sn_{0.12}$ QW device in this work achieves the lowest SS of 15 mV/dec among the compared devices [26], [27], [28].

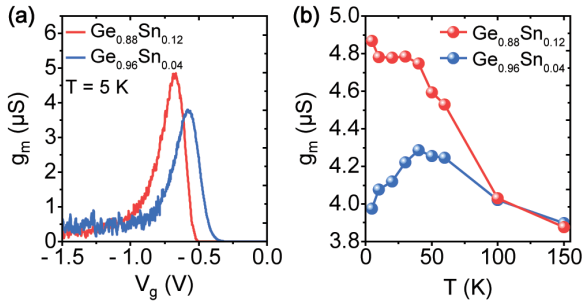

Fig. 5. (a) Transconductance g_m as a function of gate voltage for the $Ge_{0.88}Sn_{0.12}$ and $Ge_{0.96}Sn_{0.04}$QW devices measured at 5 K. (b) Temperature dependence of the measured peak g_m for both devices.

inflection phenomenon caused by the localized band-tail states [7]. In contrast, the measured SS-I_d curve of the $Ge_{0.88}Sn_{0.12}$ device closely follows the calculated results, demonstrating a reduced band-tail effect.

Previous studies have reported that increasing Sn content can lead to degraded SS due to a higher density of interface traps at the oxide/GeSn interface [21]. However, in this work, the $Ge_{0.88}Sn_{0.12}$ QW device exhibits both a monotonic reduction of the SS and a weak inflection. This behavior is attributed to strong quantum confinement in the QW and the spatial separation of the channel carriers from the gate dielectric interface, which reduce the influence of interface trap states (D_{it}) and disorder-induced band-tail states, thereby improving SS across the entire temperature range and mitigating low-temperature SS saturation. This interpretation is further supported by the C_{GC}-V_g characteristics shown in Fig. 3(c). The blue curve exhibits pronounced dual-channel behavior in the $Ge_{0.96}Sn_{0.04}$ QW device, indicating partial inversion in the top Ge layer and increased carrier proximity to the oxide interface. This suggests that the QW is not sufficiently deep to effectively confine carriers within the GeSn layer, as shown in Fig. 3(d), resulting in enhanced carrier interaction with the oxide interface. As a result, electrostatic coupling to interface-related states is enhanced, which increases the SS and leads to premature SS saturation. In contrast, the red curve in Fig. 3(c) exhibits capacitance saturation at higher V_g consistent with stronger hole confinement within the deeper GeSn QW shown in Fig. 3(d). As a result, the $Ge_{0.88}Sn_{0.12}$ QW device exhibits reduced interface-trap coupling and weaker band-tail effects compared with the $Ge_{0.96}Sn_{0.04}$ QW device, owing to the stronger quantum confinement and improved spatial separation of carriers from the HfO_2/semiconductor interface. Consequently, despite its planar device geometry, the $Ge_{0.88}Sn_{0.12}$ QW pMOSFET achieves the lowest SS reported for Ge-based pMOSFETs at temperatures below 10 K, owing to the well-confined QW channel enabled by the high Sn content [26], [27], [28], as shown in Fig. 4.

Although a significantly reduced SS has been achieved, the minimum SS remains above the theoretical Boltzmann limit (~1 mV/dec at 5 K). This deviation is primarily attributed to the Schottky barrier formed at the source/drain interfaces, resulting from the direct NiGeSn contacts on the undoped GeSn channel. Although this barrier is sufficiently low to allow efficient carrier injection in the on-state, it remains non-negligible in the subthreshold regime at 5 K. In the $Ge_{0.96}Sn_{0.04}$ QW device, the gradual increase of SS at small I_d may also be partly attributed to a relatively larger Schottky barrier [24] at the source/drain contacts, in addition to the poor QW confinement-induced localized band-tail states. Future optimization through source/drain doping is expected to further suppress this barrier and approach the theoretical limit.

Figure 5(a) presents the transconductance (g_m) as a function of gate voltage at 5 K for both devices. A higher maximum g_m is obtained in the $Ge_{0.88}Sn_{0.12}$ device, indicating an enhanced hole mobility. The temperature dependence of the peak g_m for both devices is summarized in Fig. 5(b). With decreasing temperature, the dominant scattering mechanism is expected to transition from phonon scattering to Coulomb scattering [29]. For the $Ge_{0.96}Sn_{0.04}$ QW device, the partial inversion of the Ge cap layer places carriers close to the HfO_2/Ge interface, leading to stronger Coulomb scattering from interface defects and pronounced mobility degradation at cryogenic temperatures, which results in a significant drop in g_m. In contrast, the $Ge_{0.88}Sn_{0.12}$ QW device benefits from stronger quantum confinement within the buried GeSn channel, spatially separating carriers from interface defects and thereby suppressing Coulomb scattering, resulting in a maintained or slightly enhanced g_m. It is worth noting that the increase in source/drain resistance due to Schottky contacts at cryogenic temperatures may partially limit the observable extrinsic g_m in both devices.

IV. Conclusion

In this work, GeSn QW MOSFETs are demonstrated for cryogenic operation. QW confinement spatially decouples the channel from the gate dielectric, strongly suppressing band-tail-dominated transport. Increasing the Sn content further enhances hole confinement via the elevated valence-band edge, reducing carrier interaction with defect-related states and producing a sharper turn-on. As a result, the $Ge_{0.88}Sn_{0.12}$ device exhibits a continuously decreasing SS down to 15 mV/dec at 5 K, together with enhanced g_m. These results position high-Sn GeSn QW MOSFETs as a promising platform for steep-slope, low-power Cryo-CMOS technologies.

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